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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/671,633	09/29/2003	Daisaburou Nakai	Q77670	6242

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EXAMINER	
DINH, DUC Q	

ART UNIT	PAPER NUMBER
2629	

DATE MAILED: 11/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/671,633	NAKAI ET AL.	
	Examiner	Art Unit	
	DUC Q. DINH	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 September 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) *13-33* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,6,10 and 11* is/are rejected.

7)☒ Claim(s) *2-5,7-9 and 12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This is response to the Amendment filed on September 14,2006.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kurashima et al. (U.S Patent No. 6,954,184), hereinafter Kurashima, in view of Nakagaki et al. (U.S Patent No. 6,104,370).

In reference to claim 1, Kurashima discloses an apparatus for driving a plurality of display units in a mobile electronic apparatus (col. 1, lines 62-65; Fig. 6), each including a plurality of data lines (15a, 15c), a plurality of scan lines (15b, 15d) and a plurality of pixels (75) each provided at one of said data lines and one of said scan lines (col. 11, lines 47-50), comprising:

at least one of a common data driver circuit (67a) and a common scan driver circuit (a data-line drive IC 67a and scanning-line drive ICs 67b are provided. The scanning-line drive ICs 67b are provided at both sides of the IC mounting area (one for each side), while the data-line drive IC 67a is provided therebetween. The data-line drive IC 67a supplies image signals to the line wires 73 of the main display 1B and to the line wires 83 of the sub-display 2B. The scanning-line drive ICs 67b supply scanning signals to the second electrodes 15b of the main display 1B and to the fourth electrodes 15d of the sub-display 2B; col. 13, lines 14-23).

Accordingly, Kurashima discloses everything except said common data driver circuit including a plurality of first switch groups, each first switch group being connected to the data lines of one of said display units for driving the data lines of said one of said display units, said common scan driver circuit including a plurality of second switch groups, each second switch group being connected to the scan lines of one of said display units for driving the scan lines of said one of said display units.

Nakagaki discloses first switch groups (33b) each first switch group being connected to the data lines (35) of the said display (31) for driving the data lines of the display 31, and a second switch groups (42), each second switch group being connected to the scan lines (34) of display unit (31) for driving the scan lines of said display unit (31; Fig. 6; col. 5, lines 9-18).

It would have been obvious for one of ordinary skill in the art at the time of the invention to provide the first switch groups for driving data lines of one of the display and second switch groups in the displays of Kurashima as taught by Nakagaki because the first switch groups would control the output of the video signals to the signal lines and the second switch groups would control the output of the scanning signal provide for the gate lines of the display units (col. 5, lines 9-18 of Nakagaki).

In reference to claim 11, Nakagaki discloses the scan driver 41 further includes a plurality of fourth switch groups (43) each fourth switch group being connected to the scan lines (34) of said display units for supplying an off-level voltage to the scan lines of the display unit (31) (col. 5, lines 63-67 and col. 6, lines 1-3 of Nakagaki).

It would have been obvious for one of ordinary skill in the art at the time of the invention to provide the switch groups (43) to turn off the level voltage to the scan lines of the display unit

in the device of Kurashima because it would provide a switch group to turn off the signal provide to the scan lines when the display is set in the right scanning mode (col. 5, lines 63-67 and col. 6, lines 1-3 of Nakagaki).

3. Claims 6 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kurashima and Nakagaki as applied to claims 1 and 11 above, and further in view of Ohtani et al. (U.S Patent No 6,826,014).

In reference to claim 6, the combination of Kurashima and Nakagaki discloses everything except the data driver circuit comprises a shift register circuit for shifting a horizontal start signal in accordance with a horizontal clock signal; a line memory, connected to said shift register circuit, for storing one line data in accordance with said shift register circuit; a gradation voltage generating circuit; a decoder circuit, connected to said line memory and said gradation voltage generating circuit, for selecting gradation voltages from said gradation voltage generating circuit in accordance with output signals of said line memory; and an output circuit, connected between said decoder circuit and said first switch groups, for transmitting said selected gradation voltages to said first switch groups, so that said selected gradation voltages are transmitted to the data lines of one of said display units in accordance with the operations of said first switch groups.

Ohtani discloses a data driver (300 in Fig. 1) comprising a shift register circuit (301) for shifting a horizontal start signal (STR) in accordance with a horizontal clock signal (CL); a line memory (302) connected to said shift register circuit (301), for storing one line data in accordance with said shift register circuit (301); a gradation voltage generating circuit (200); a decoder circuit (304), connected to said line memory (302) and said gradation voltage generating

circuit (200), for selecting gradation voltages from said gradation voltage generating circuit in accordance with output signals of said line memory (302); and an output circuit (305), connected between said decoder (304) for transmitting said selected gradation voltages so that said selected gradation voltages are transmitted to the data lines of one of said display units (see Fig. 1, col. 7, lines 1-64).

It would have been obvious for one of ordinary skill in the art at the time of the invention to modify the common data driver (300) in the combination of Kurashima and Nakagaki as taught by Ohtani because it would provide a high-quality display, and reliability of a liquid crystal can be enhanced (col. 1, lines 20-25).

In reference to claim 10, the combination of Kurashima and Nakagaki discloses everything except the scan driver comprising a shift register circuit for shifting a vertical start signal in accordance with a vertical clock signal and an output circuit, connected to said shift register circuit, for transmitting output signals of said shift register circuit to said second switch groups, so that the scan lines of one of said display units are sequentially scanned by said second switch groups.

Ohtani discloses a scan driver circuit (400; Fig. 1) comprising a shift register circuit for shifting a vertical start signal (GST) in accordance with a vertical clock signal (GCL) and an output circuit, connected to said shift register circuit for transmitting output signals of said shift register circuit to the scan lines (Fig. 1; col. 7, lines 65-67 and col. 8, lines 1-9).

It would have been obvious for one of ordinary skill in the art at the time of the invention to provide the use of the shift register circuit and output circuit in the combination of Kurashima

and Nakagaki as taught by Ohtani thereby the TFTs connected to each gate line successively turn ON, the display data signal supplied to each data line from of the data driver is supplied to the liquid crystal display pixel, and an image display operation is performed (col. 8, lines 4-10).

Response to Arguments

Applicant's arguments filed September 14, 2006 (see the Reamarks) have been fully considered but they are not persuasive. As discussed above, Kurashima discloses the common data driver and common scan driver for driving the main display 1B and the sub-display 2B but does not provides the first groups of switches for control the one of the data lines and second groups of switches to control the driving of one of the driving circuit. Therefore, it would have been obvious for one of ordinary skill in the art at the time of the invention to provide the first switch groups for driving data lines of one of the display and second switch groups in the displays of Kurashima as taught by Nakagaki because the first switch groups would control the output of the video signals to the signal lines and the second switch groups would control the output of the scanning signal provide for the gate lines of one the display units (col. 5, lines 9-18 of Nakagaki).

4. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies are not recited in the rejected claim(s). [switches used to switch ton ones of the main and sub-displays, i.e., ... as set fort by the claim because data would not need to be switched to one of the main and sub-display. It is note that the claim 1 recites groups of first and second switches are used for driving scan lines and data lines of on of the display units]. Although the claims are interpreted in light

of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Therefore, the rejection is maintained.

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Allowable Subject Matter

6. Claims 2-5, 7-9 and 12 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: none of the cited arts teaches or suggests:

said common data driver circuit comprises: a plurality of frame memories for storing video signals, each for one of said display units; a plurality of third switch groups each group being connected to one of said frame memories and being operated in synchronization with operations of said first switch groups (claim 2).

said gradation voltage generating circuit comprises a plurality of gradation voltage generating units each for one of said display units (claim 7).

"a plurality of first switches each connected to one of said voltage followers; and a plurality of second switches each connected between an input of one of said voltage followers and an output of one of said first switches, wherein said first switches are turned ON for a first predetermined time period, and then, said second switches are turned ON while said first switches are turned OFF (claim 8).

frequency control circuit, connected to said fifth and sixth switch groups, for selecting and turning ON one switch of said fifth switch group and one switch of said sixth switch group, so that the data lines of said one of said display units are driven by a selected one of said horizontal clock signals and the scan lines of said one of said display units are driven by a selected one of said vertical clock signals, thus always realizing a definite frame frequency of said one of said display units (claim 12).

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to DUC Q. DINH whose telephone number is (571) 272-7686. The examiner can normally be reached on Mon-Fri from 8:00.AM-4:00.PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Hjerpe can be reached on (571) 272-7691. The fax phone number for the organization where this application or proceeding is assigned is **571-273-8300**.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DUC Q DINH
Examiner
Art Unit 262929

DQD
November 17, 2006

RICHARD HJERPE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600